

ATTACHMENTS

- i. **Page 5** of the Detailed Description
- ii. **FIG. 2** of the Drawings
- iii. **Pages 1 - 4** of a Restriction Requirement Mailed 09/11/2002 and stating the now Waived objections to **FIG. 2**.

AUTHORIZATION TO CHARGE FEES DUE TO THE HP PTO DEPOSIT

ACCOUNT #: 08-2025

Applicant hereby authorizes any fees due to be charged to the Hewlett-Packard PTO Deposit Account Number: **08-2025**.

CONCLUSION

Based on the foregoing, the Applicants respectfully request that the PTO accept Applicants timely payment of the Issue Fee for application serial number **09/934,548**.

Respectfully submitted,

Ping Mei

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By: 

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1 materials can be used to form the substrate 160 because of the relatively low temperature
2 fabrication method used to produce the memory device 10.

3 The data lines 130 can be thin strips of semiconductor material, such as silicon.
4 The data lines 130 can be deposited as a silicon layer over the substrate 160, which can be
5 subsequently patterned to form the data line 130 strips. The silicon can be an amorphous
6 silicon deposited by, for example, plasma enhanced chemical vapor deposition (PECVD).
7 Alternatively, the silicon strips can be polycrystalline silicon, crystalline silicon, or
8 semiconductors such as SiGe, Ge, SiC, GaAs, and organic semiconductors. The data
9 lines 130 can have a thickness on the order of, for example, 1000 Angstroms. The
10 thickness of the data lines 130 may vary according to the material used to form the data
11 lines 130.

12 The p-channel TFTs 170 may be used as resistive load elements for the memory
13 array 100. The p-channel TFTs 170 may be synchronized with gate line pulses to the
14 memory cells 200, and provide power savings during idle periods for the memory device
15 10. The p-channel TFTs 170 can be replaced with, for example, a simple n-channel
16 circuit, or, a resistive circuit.

17 The structure of the memory cells 200 is discussed in detail with reference to
18 Figures 3A and 3B.

19 Figure 3A is a sectional view taken along the section line 3-3 in Figure 2, of a
20 TFT memory cell 200 before a write operation. Neighboring memory cells 200 on the
21 data line 130 are also illustrated. Figure 3B is a sectional view taken along the section
22 line 3-3 of the memory cell 200, after a write operation.

23 The memory cell 200 is a three terminal transistor device. The memory cell 200
24 may be a thin film transistor formed at the intersection of a gate line 110 and a data line
25 130. The memory array 100 may therefore include a number of memory cells 200 equal
26 to the number of intersections of the gate lines 110 and the data lines 130.

27 The memory cell 200 comprises a channel region 132 of the data line 130, a
28 source region 134 of the data line 130, a drain region 136 of the data line 130, a gate
29 insulator 211 having a gate insulator layer 212 disposed over the channel region 132 and
30 a gate insulator layer 216 disposed over a floating gate 214, and a gate line 110 extending
31 over the gate insulator 212. The portion of the gate line 110 contacting the gate insulator
32 216 serves as a gate electrode 218 for the TFT memory cell 200.

33 The gate insulator layers 212, 216 may be layers of dielectric material. The gate
34 insulators 212, 216 may be separate layers on either side of the floating gate 214, as



T¹ THIN FILM TRANSISTOR MEMORY DEVICE

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FIG. 1

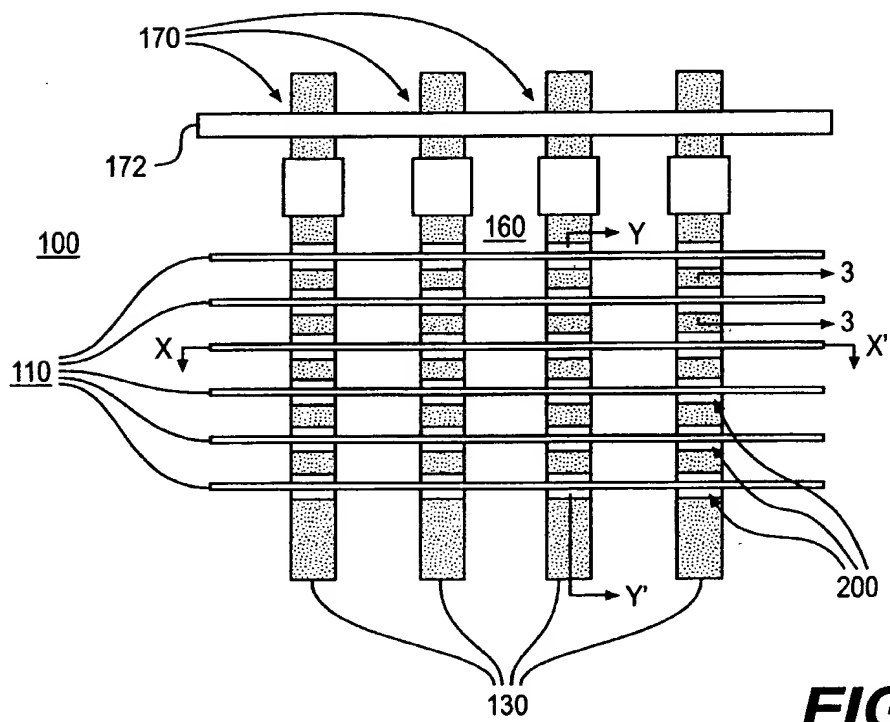
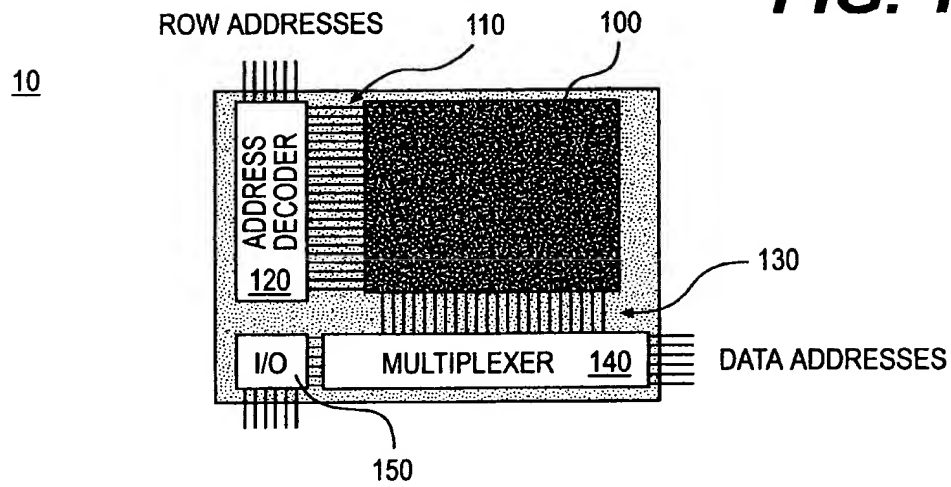


FIG. 2